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How flat is the flatband potential?†

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The development of semiconductor devices requires extensive effort dedicated to the interface characterizations. However, these measurements can be affected by defects. As a consequence, the experimental results can fall off from theoretical consideration, *e.g.* the electron affinity rule, and the interpretation and the manipulation of quantities such as the flatband potential (V_{fb}), the built-in voltage (V_{bi}) and the thermionic voltage (V_{th}) can be confusing. This article highlights that these issues can be solved in considering the surface potential ($V_{surf.}$) relationship with the bulk potential (V_{bulk}), *i.e.* the space charge region (SCR). The findings are based on results obtained on Si/SiO_2 interfaces by photoelectron spectroscopy (PES) and electrical measurements suggesting a defect-induced volt range $V_{surf.}$ drop within few nanometers. This can lead to the measurements of negative V_{fb} and dispersive V_{fb} values over several volts. Finally, the interpretation of the experimental data shows that the V_{fb} corresponds to a maximum drop in $V_{surf.}$ for a flat V_{bulk} in the presence of shallow interfacial defects in the semiconductor bandgap. The outcomes of this article can provide valuable inputs in the manipulation of the abovementioned quantities while it is proposed to include a defect-driven $V_{surf.}$ term in the electron affinity rules to account for the observed experimental deviations.

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1 Introduction

The development of semiconductor devices is accompanied by the characterization of interfaces through specific quantities. They can be the flatband potential,[1] the built-in voltage,[2–4] the thermionic voltage,[5] the barrier height,[6] the Schottky barrier[7,8] and the band-bending[6] with all of them finding applications either in solid-state devices such as in solar cells,[2,3,5] semiconductor–metal contact[8] semiconductor-oxide heterostructures,[4] thermionic devices[7] or in photo-electrochemical devices.[1,6] In this article, three quantities are used to limit lexical redundancy and to have a more complete description of the semiconductor interface properties: the flatband potential (V_{fb}), the built-in voltage (V_{bi}) and the thermionic potential (V_{th}).

Such interface investigations are necessary and motivated for comparing and optimizing the performance and the efficiency of semiconductor devices, especially when used for energy applications. For instance, larger V_{bi} values can be required for having an efficient electron–hole pair separation as a result of a decrease in charge recombination at the interface of a photo-active material.[9] As a consequence, larger V_{bi} are desired for increasing the photo-current, the open circuit voltage and the energy light conversion efficiency of solar cell devices.[3,9] A similar statement can be formulated for the photo-electrochemical devices: larger V_{bi} values are beneficial to the generated photoelectrochemical-current and the energy light conversion efficiency.[6]

In this prospect, as a theoretical tool, a scientist can employ the Anderson's rule,[10] also known as the electron affinity rule for estimating the energy band-alignment and the properties of an interface of a device under design.[11] This rule states that the energy band-alignment at the interface and the V_{bi} are driven by the workfunction differences of the contacted materials. Although it is not a completely satisfactory theory and could be even controversial,[12] most experimental works on solid-state or photoelectrochemical devices follow this logic. The deviation from the theory is often attributed to imperfect interfaces leading to undesired Fermi Level Pinning (FLP).[8,13–15] The FLP is a phenomenon which is observed with a wide class of semiconductor materials and empirical theories have been developed for completing the electron affinity rule.[11] FLP is particularly strong for the covalent III–V and the elemental semiconductors (*e.g.*: Si, GaAs, CdTe, InP)[11,13] as well as halide perovskite[16–18] but it could be less prevalent in II–VI chalcogenides and oxide semiconductors.[11,13] It is generally higher with covalently-bonded than ionically-bonded semiconductors.[8,11,13]

Also, the literature reports some difficulties in the measurements, the manipulation and the interpretations of derived quantities from the interface characterizations.[19–24] Thus, the V_{fb} determination from the Mott–Schottky plot has been a topic of discussion in recently published articles dealing with photo-electrochemical devices.[19,20,24] Concurrently, the V_{fb}

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can be indistinctly confounded with the V_{bi} and, to the best of the author knowledge, there is no proof for any correlations between the V_{th}, the V_{bi} and the V_{fb} in the literature.

In this context, this study aims at bringing a contribution on the understanding and the manipulation of the mentioned quantities. The experiments are performed by X-ray PES experiments (information depth < 10 nm) on hydrogen plasma treated n-Si(100)/(2.5 nm)SiO_2 substrates abbreviated as Si/SiO_2 throughout this article and electrical experiments. The PES measurements strongly suggest the presence of a defect induced volt range $V_{surf.}$ which screens the top few nanometers and affecting both the silicon subsurface and the SiO_2 layer. Complemented with the electrical measurements, which reports a negative V_{fb}, the potential distribution mechanism between V_{bulk} and $V_{surf.}$ in the presence of shallow interfacial defects is detailed. Also, its implications on the V_{fb}, V_{bi}, V_{th} and the electron affinity rule are discussed. In particular, it is assumed that the V_{fb} is not as flat as it can be and can actually be a potential corresponding to a maximum in $V_{surf.}$ for a flat V_{bulk} in the presence of shallow interfacial defects.

2 Experimental

2.1 Sample preparation

Ohmic n^+-rich back contact and tunneling Si/SiO_2 front contact are fabricated from 3″ inch n-type float-zone silicon single crystal (100) wafer (sheet resistivity: 10 Ω cm, donor concentration N_d: 10^{14} cm^{-3} range). First, the wafer is chemically cleaned in a piranha bath (H_2O_2 : H_2S_4 5 : 2) followed by a fluoridic acid (HF 2%). An extensive di-ionized (DI) water rinsing is realized after each bath. Second, a thick 200 nm-sacrificial SiO_2 layer is deposited on one side of the silicon wafer. Third, phosphor diffusion is performed at 900 °C for 5 min under nitrogen which results in the formation of n^+-rich region on the unprotected side of the wafer. Fourth, again a piranha bath and a 2% HF bath followed by DI rinsing are realized before a tunneling 2.5 nm thick SiO_2 layer and a poly-silicon glass (PSG) are thermally grown in a Koyo VP1000 furnace on the H-terminated front contact and the n^+-rich back contact, respectively. The wafer is then diced into 10 × 10 mm pieces and a platinum metallic contact is deposited on the n^+-rich side by sputtering. The ohmic back contact is validated by Electrochemical Impedance Spectroscopy (EIS) (see Fig. S1†). SiO_2 thickness and homogeneity is assessed by comparing the photoemission intensity of the oxide over the elemental silicon at different sample angles in the PES chamber.[28,29] It is worth noting that the Si/SiO_2 transition grown at elevated temperature must be abrupt and about 1–2 monolayer thick.[30,31]

The samples are then inserted in the DArmstadt's Integrated SYstem for MATerial Science (DAISY-MAT) where they can be manipulated and transferred between the hydrogen plasma source, the sputtering chambers, the atomic layer deposition chamber and the PES platform without breaking the high vacuum level preventing external sample contamination such as water and hydrocarbon species (see Fig. S2†).[32]

Before any experiments in the DAISY-MAT system, the Si/SiO_2 front side of the samples are exposed to a hydrogen plasma source (Tectra Gen2 Hybrid Atom/Ion Source) for 45 min at 350 °C. The plasma source is set on atomic mode with the current as 30 mA and the gas pressure as 0.2 mbar. To avoid possible hydrogen desorption from the sample, the plasma is maintained until the substrate temperature is cooled down to 150 °C. The hydrogen plasma eliminates carbonate species on the surface (see Fig. S3†) and it is believed to passivate the Si/SiO_2 interface.[33–38]

2.2 Alumina atomic layer deposition (ALD)

ALD-alumina was deposited by the alternative deposition and oxidation by water of trimethylaluminum (TMA) at different temperatures. TMA and water pulses lasted for 80 and 150 ms, respectively, and were separated by an evacuation period of 5 min.[39] Numerous ALD programs have been tested where the first pulse composition (water or TMA), temperature and number of cycles were varied. A list of the different prepared samples are available in the Table S1 of the ESI.† After the ALD deposition, another hydrogen plasma step was realized as described above.

2.3 Sputtering deposition

The sputtering deposition during the interface experiments is realized by direct current sputtering on the hydrogen plasma treated Si/SiO_2 samples without breaking the vacuum. Platinum (Pt) is deposited at 5 W, from room temperature (RT) to 325 °C, in an argon atmosphere at 1–6 Pa and with a target to substrate distance of 7.5 cm. Although varied, no significant influence of the explored Pt deposition conditions has been observed on the behaviors of the final structure. For this reason, the temperature and the pressure during the Pt deposition are not indicated in the article. The nickel oxide (NiO) layer is deposited by Metal Layer Oxidation (MLO), which consists in separating the stage of deposition to the stage of oxidation for avoiding the formation of oxygen interstitial in the Si/SiO_2 interface[40] during sputtering. MLO is prepared from a nickel metallic target at 1 Pa in an oxygen free atmosphere and is followed by an oxidation step in the presence of oxygen at 1–6 Pa either at room temperature (RT) or higher temperature (HT) when prepared between 100 °C and 200 °C. As detailed in a previous article, PES measurements show that the NiO layer prepared by MLO is conform to standard NiO layers.[40]

2.4 Interface and bias assisted electron exposure experiments

All X-ray PES measurements are realized in a Physical Electronics PHI 5700 multitechnique chamber with a Al Kα monochromatic X-ray ($h\nu$ = 1486.6 eV) source. The substrate to the detector angle is 45° and the PES chamber pressure during the measurements is in the 10^{-8} to 10^{-9} torr range. For the data correction, the Fermi level (E_F) in the chamber was recorded on a clean silver surface beforehand.

As represented in Fig. S4,† the interface experiments consist in transferring the Si/SiO_2 samples from a sputtering deposition chamber to the PES chamber without breaking the high vacuum conditions. PES measurements are therefore recorded *in situ* for

a stepwise thickness increment of a fraction of a nanometer of deposited materials (Pt or NiO) in the sputtering chamber.[32]

Bias-assisted electron exposure (BAEE) experiments were performed on the hydrogen plasma treated Si/SiO_2 samples and consisted in applying a bias potential from 0 V to 4 V under an electron flux during the X-ray PES acquisition (see Fig. S4†). The electron flux is generated by an electron gun (neutralizer) at 24 mA and 20% of maximum power. As described elsewhere, such setup configuration can be used for pseudo-operando characterizations.[41,42] The BAEE data are potential corrected for being compared with the data collected during the interface experiments (see Fig. S5†).

PES quantities such as the full width at half maximum (FWHM) and peak position are extracted after Shirley background subtraction.

2.5 Electrical measurements

Electrical measurements have been performed on Pt terminated Si/SiO_2 Schottky contact from which about 2 mm of the 10 × 10 mm samples are cleaved along each edges. It aims at reducing leakage current from the front to the back side of the device. The surface area is determined with the software ImageJ. Electrochemical impedance spectroscopy (EIS) and current–voltage (I–V) measurements are then performed in the dark. The EIS measurements are performed with an Agilent 4294A impedance analyzer from 40 Hz to 10 MHz at different bias potential in a four-probes configuration terminal. The I–V curves were obtained with an Agilent 4156C semiconductor parameter analyzer in a two-probes configuration from −1 V to 0.5 V. Although the connectors were not absolutely the same, it has been assumed that the value of the contact resistance (R_c) estimated by EIS could be used for a R_c post-correction of the experimental I–V measurements, following: $V_g = V_{g,exp} - iR_c$ where i is the current during the measurement and $V_{g,exp}$ the experimental bias.

3 Results and discussion

As described in Fig. 1a, following the electron affinity rule, a Schottky contact realized with a n-type semiconductor and a higher workfunction metal must lead to the creation of a space charge region (SCR) in the semiconductor, characterized by a theoretical built-in voltage (V_{bi}^*):

$$qV_{bi}^* = \phi_m - \phi_{sc} \quad (1)$$

where q is the elementary charge, ϕ_m and ϕ_{sc} are the workfunction of the contact material and the semiconductor, respectively. The experimental V_{bi} being smaller than or equal to the theoretical V_{bi}^* because of the FLP. In this article, it is stated that the V_{bi} is a bulk quantity and screening the top first μm of the silicon under the interface, contrary to the $V_{surf.}$ being a surface quantity and screening only few nm around the Si/SiO_2 interface.

Fig. 1b shows the recorded PES spectra with the Si^0 peak (98–101 eV) and the Si^{IV} peak (101–106 eV) corresponding to the photoelectron emission from the elemental silicon (Si) and the silicon dioxide (SiO_2), respectively.[43] The obvious Si^0 and Si^{IV} peaks separation enables to evaluate the interface properties through different layers, which would be less straightforward for a homogeneous interface.

The photoelectron emission measurements recorded without breaking the vacuum during the interface experiments with platinum (Pt), nickel oxide (NiO), alumina (Al_2O_3) and during the bias assisted electron exposure (BAEE) experiments displays shifted Si^0 peaks to lower binding energy for any experiments. This can be interpreted as the result of a bulk potential (V_{bi}) in the silicon or/and a surface potential ($V_{surf.}$) at the Si/SiO_2 interface. Indeed, the measured kinetic energy ($E_k(x,y,z)$) of the photoemitted electron is affected by the local potential ($V(x,y,z)$) within the probed material following:

$$E_k(x,y,z) = h\nu - E_{BE}^* + qV(x,y,z) \quad (2)$$

with $h\nu$ the photon energy and E_{BE}^* the theoretical electron binding energy. However, as observed in Fig. 1b, the Si^0 shift is accompanied by a considerable variation from 4.2 eV to 3.8 eV of the peaks separation $\Delta Si = Si^{IV} - Si^0$ which cannot, be attributed to a V_{bi} only. Indeed, the calculation shows that the electric field in the SCR in the n-type silicon cannot exceed more than 10^6 V m^{-1} near the Si/SiO_2 interface which corresponds to a potential drop of 1 mV nm^{-1}. With an information depth of few nanometers, the PES measurements should not be exposed to any substantial potential variation implied by the V_{bi}, *i.e.* the SCR. Therefore, it is proposed that the observed variation find an origin in the built-up of $V_{surf.}$ at the Si/SiO_2 interface. To explore this assumption, as represented in Fig. 1c, four $V_{surf.}$ profiles across the Si/SiO_2 interface have been incrementally investigated. The Case i is generated by a constant electric field in the $\pm 10^9$ V m^{-1} range and screens the SiO_2 layer only. The Case ii is generated by charges ($\pm 10^{19}$ cm^{-3}) located in the top 1.5 nm of the silicon subsurface only. The Case iii describes a $V_{surf.}$ generated by a similar charges density to the Case ii but they are located in the top 5–6 nm of the silicon subsurface and the potential in the SiO_2, considered charge-free, is derived from the electric field (E) continuity at the Si/SiO_2 interface:

$$\varepsilon_{SiO_2} E_{Si} = \varepsilon_{Si} E_{SiO_2} \quad (3)$$

with $\varepsilon_{Si} = 11.7$, $\varepsilon_{SiO_2} = 3.9$ which are the relative permittivity of the silicon and the silicon dioxide, respectively.[44] Eventually, the Case iv is a combination of the Case iii and a dipole located at the Si/SiO_2 interface which causes a sharp potential drop[45–47] while respecting the electric field continuity condition in eqn (3).

These four $V_{surf.}$ profiles are assumed to generate a PES fingerprint and can be simulated in integrating the photoelectron intensity along the depth z following:

$$I_{meas}(E_{BE}) = \int_0^\infty I_{id}(E_{BE} - qV(z))\exp(-z/\lambda)dz \quad (4)$$

where I_{meas} is the resulting photoemission intensity along the binding energy E_{BE}, I_{id} is an ideal spectra shifted by the potential $V(z)$ in a material characterized by an inelastic mean

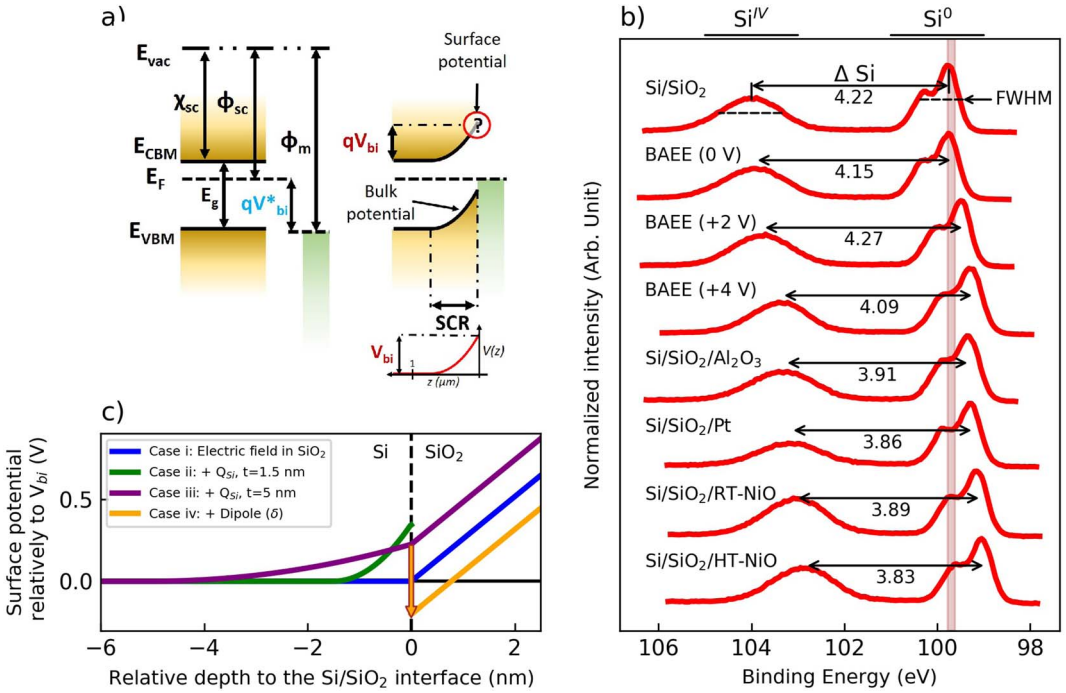

Fig. 1 (a) Band-diagram representation of a typical n-type semiconductor/metal band-alignment before and after contact along the depth z. E_F, E_{vac}, E_g, E_{VBM}, E_{CBM} and χ_{sc} are the Fermi level, the vacuum energy, the bandgap, the valence band maximum, the conduction band minimum of the semiconductor and the electron affinity, respectively.[8,25–27] The SCR and the surface potential region are in the μm and nm range, respectively. (b) Si 2p spectra recorded on the Si/SiO_2 substrates during the PES interface experiments with alumina (Al_2O_3), platinum (Pt), room temperature nickel oxide (RT-NiO), high-temperature nickel oxide (HT-NiO) and also during bias assisted electron exposure (BAEE) experiments. The vertical brown line represents the position of the Si^0 peak after the hydrogen plasma treatment for a series of nine samples. The peak separation $\Delta Si = Si^{IV} - Si^0$, absolute peak position and the full width at half maximum (FWHM) are the derived quantities from the PES measurements. (c) Investigated $V_{surf.}$ models for explaining the peak distortions recorded in the Si 2p region by PES on the Si/SiO_2 substrates. The vertical arrow represents the dipole discontinuity.

free path (IMFP) factor λ.[48] More details on the PES simulation are available in the Section S2 of the ESI.†

Fig. 2 displays the experimental and the simulated PES data in the Si 2p region along with electrical measurements on identical Pt terminated Schottky junction providing important observations for understanding the V_{bulk} relationship, *i.e.* the SCR, with the $V_{surf.}$. Fig. 2a and b compares the full width at half maximum (FWHM) of the Si^0 according to its absolute position and the FWHM of the Si^{IV} peak according to the peak separation ΔSi, respectively. The simulated PES data are obtained with varying electric field (Case i), varying charges (Case ii and Case iii) while the dipole is considered to shift horizontally the simulated data in Fig. 2b proportionally to its intensity (Case iv). In the meantime, Fig. 2c shows the Mott–Schottky curves of the Pt terminated Schottky device and Fig. 2d aims at comparing V_{th} and V_{bi} according to V_{fb}. These quantities were previously extracted from the EIS and *I–V* measurements on Pt terminated Schottky devices. Thus, V_{fb} is determined following the Mott–Schottky equation[49,50] which is for a n-type semiconductor:

$$\frac{1}{C_{scr}{}^2} = \frac{2}{qN_d\varepsilon\varepsilon_0 S^2} \times (V_{fb} - V_g) \quad (5)$$

with C_{scr} the capacitive element related to the SCR in the semiconductor, N_d the donor density, S the contact area, V_g the bias potential, ε the material relative dielectric permittivity and ε_0 the vacuum permittivity. V_{bi} is determined from the value of the induced capacitance in the SCR under zero current conditions in the dark, which is obtained for $V_g = 0$ V for the studied solid-state device:

$$V_{bi} = \frac{qN_d\varepsilon\varepsilon_0}{2\left(\frac{C_{scr}{}^{V_g=0V}}{S}\right)^2} \quad (6)$$

This definition is not commonly adopted but it is introduced as a relevant method for determining V_{bi} with regards to the outcomes of this article. Finally, V_{th} is related to the thermionic emission at the semiconductor interface.[51–54] Under the presence of an external bias V_g, the current density j_{total} follows the diode equation:

$$j_{total} = j_0\left(e^{\frac{qV_g}{\eta k_B T}} - 1\right) \quad (7)$$

where η is the diode ideality factor, T the temperature in kelvin, k_B the Boltzmann constant and j_0 the exchange current density which is:

$$j_0 = A^*T^2 e^{-\frac{\phi_{th}}{k_B T}} \quad (8)$$

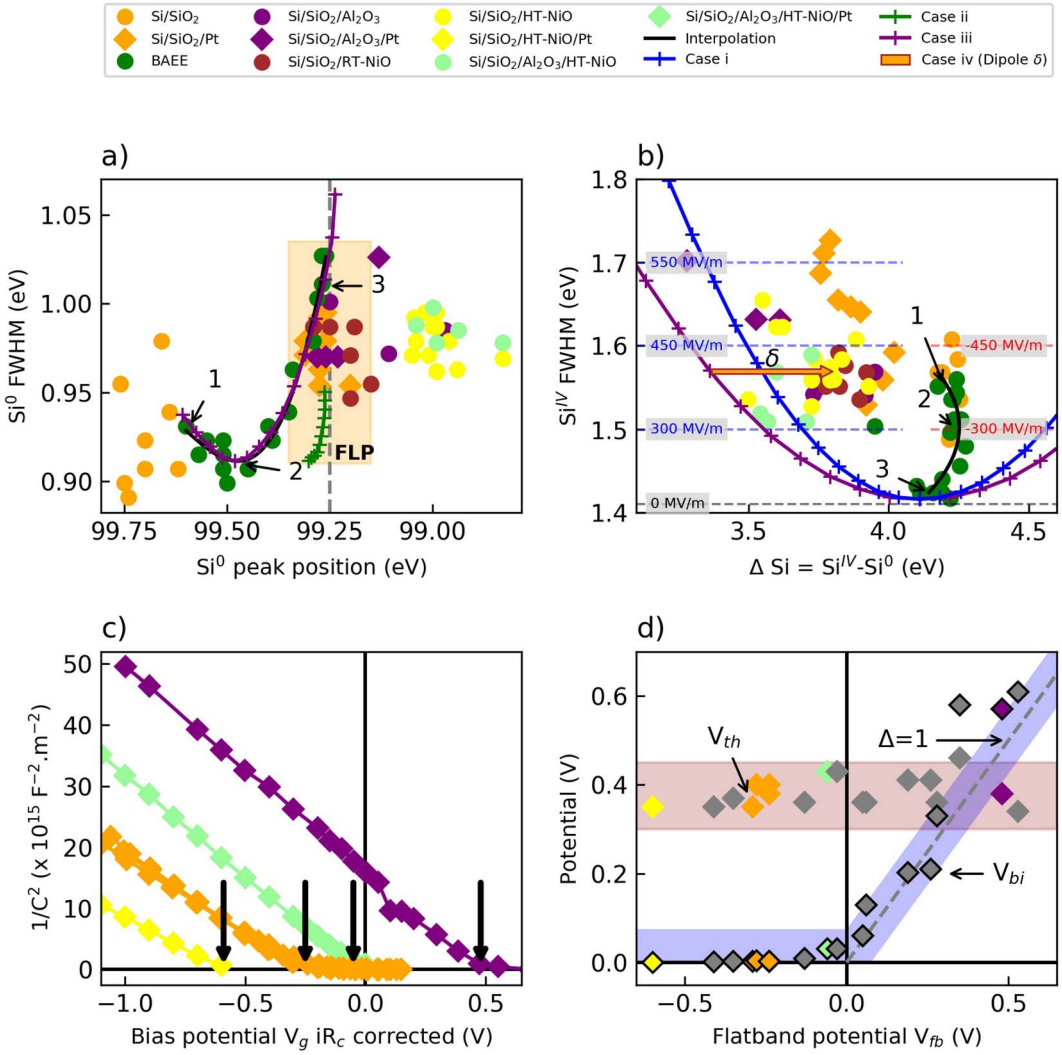

Fig. 2 (a) Si^0 full width at half maximum (FWHM) according to its absolute binding energy position as measured by PES (see Fig. 1b), (b) FWHM of the Si^{IV} peak according to ΔSi 2p peak separation. The points 1, 2 and 3 represents BAEE experiments at 0 V, +2 V and +4 V, respectively. (c) Mott–Schottky representation of the capacitive element associated to the SCR (see the Section S1.5.2 of the ESI†). The V_{fb} are indicated by vertical arrows. (d) Comparison of V_{bi} (symbols with black edges) and V_{th} (symbols without edges) with V_{fb}. The grey symbols are incorporated results obtained with differently prepared Si/SiO_2 samples contacted with Pt (see Table S1†). The symbol Δ represents a correlation equal to one for positive V_{fb}.

where A^* is the Richardson constant and $\phi_{th} = qV_{th} + (E_F - E_{CBM})$, is the barrier height at the semiconductor interface. The analysis of the measured I–V curve can enable to retrieve V_{th}. In this article, the V_{th} is determined from the I–V analysis in the 0.1–0.4 V forward bias potential. More details on the methods for extracting V_{fb}, V_{bi} and V_{th} based on the eqn (5)–(8) are available in the Sections S1.5.2 and S1.5.3 of the ESI.†

In Fig. 2a, the strongest Si^0 peak deviations in the lower binding energy relative to the bare Si/SiO_2 interface are obtained when NiO or Al_2O_3 are contacted in comparison to Pt. The deposition of a Pt overlayer on top of either the Si/SiO_2, Si/SiO_2/NiO or $Si/SiO_2/Al_2O_3$ interfaces yields to similar Si^0 peak position close to 99.25 eV. This final position unveils the presence of defects leading to the FLP when their ionization level comes across the Fermi level. The FLP at 99.25 eV is characterized with a Si^0 width increase from about 0.9 to 1 eV as observed in the course of the BAEE experiments (see point 2 to point 3 in Fig. 2a). Such width increases associated to the FLP is also reported in the frame of a study on the water absorption on a titanium oxide (TiO_2) layer by ambient-pressure X-ray PES.[55] In the meantime, as shown in Fig. 2b, the ΔSi peak separation is gradually shortened during the experiments in comparison to the bare Si/SiO_2 samples. A width minimum can be observed for both the Si^0 and the Si^{IV} peaks which are 0.91 eV (point 2 in 2a) and 1.41 eV (point 3 in 2b), respectively. These minimums are considered as corresponding to a minimal potential drop through the probed layer. It is worth mentioning that the interface experiments and the BAEE experiments enable to probe Si^0 binding energy and ΔSi peak separation regions that complement each other.

The simulated PES fingerprints of the potential profiles in Fig. 1c describes parabolic curves in Fig. 2a and b, where the

simulated data are extrapolated from ideal Si^0 and Si^{IV} peaks obtained at their respective minimum width (more details are provided in the Section S2 of the ESI†). The Case i displays a parabolic curve in the Fig. 2b only as the electric field is investigated exclusively for the SiO_2 layer. It shows that the width of the Si^{IV} peak and the ΔSi 2p variation are correlated to the electric field intensity and to the average potential in the SiO_2 layer, respectively. For instance, an increase of the Si^{IV} width from 1.4 eV to 1.5 eV can be explained by a rise from 0 to 300 MV m^{-1} of the electric field in the SiO_2 layer (see the iso-electric field line in Fig. 2b). The Case ii and iii, can explain the increase of the Si^0 width when the Si^0 peak position is close to the FLP region in Fig. 2a but the Case iii provides a relatively exact matching with the experimental data acquired during the BAEE experiments. It can therefore support the assumption that the top 5–6 nm of the silicon subsurface is screened by a potential induced by an accumulation of positive charges during the experiments which leads to the FLP. In such a case, the charge density is estimated to be about 10^{19} cm^{-3} within the top 5–6 nm of the silicon (see the Section S2 of the ESI†). However, coming back at the Fig. 2b, the parabolic curve obtained with the Case iii is larger and deviates more from the experimental data than what can be obtained with the Case i. This is because of the potential drop in the silicon layer introduced in the Case iii but not in the Case i. Therefore, as proposed in the Case iv, the contribution of a dipole at the Si/SiO_2 interface can provide an explanation for the observed difference between the simulated data in the Case iii and the experimental data (see the horizontal arrow in Fig. 2b).

Overall, the *in situ* PES measurements comparison with the simulations suggest the presence of charges in the 10^{12} cm^{-2} density range, screening the top 5–6 nm of the silicon subsurface and pinning the Fermi energy at 99.25 eV. The reported charge density range is in line with the literature[13,56] and it can originate from an ionization reaction ($D^0 \rightarrow D^+ + e^-$) of the interfacial defects leaving positive trapped charges in the vicinity of the Si/SiO_2 region. The resulting potential in the silicon subsurface is assumed to generate a potential barrier of up to 0.3–0.4 V. To the right of the FLP region in Fig. 2a, the Si^0 width is relatively constant and is about 1 eV. This could suggest that every states D^0 have been ionized and a fraction of the potential is distributed in the SCR. With respect to the eqn (3), the positive charges might induce an electric field which can reach up to 500 MV m^{-1} in the SiO_2 layer which is equivalent to a potential drop of 1.2 V. Similarly, a 1.8 V potential drop in the SiO_2 layer was also reported in the course of cesium deposition on a p-Si/SiO_2 sample.[57] Finally, the comparison of the experimental data with the simulated ones can suggest the presence of a dipole in the 0.3 to 0.6 V range located at the Si/SiO_2 interface.

From the PES analysis, it can be stated that the FLP occurs when the energy level of the interfacial defects comes across the Fermi level (E_F) leading to the formation of positive (*e.g.* $D^0 \rightarrow D^+ + e^-$) or negative trapped charges (*e.g.* $D^0 + e^- \rightarrow D^-$) which generate a surface potential. Such reactions require the implication of shallow defects which are close to the Fermi level and interact with the semiconductor bandgap, in contrast to deep defects leading to fixed charges which are too far from the Fermi level for being subjected to any reactions.[58] These reactions are expected to be reversible depending on the defect position relatively to the Fermi level. For the studied Si/SiO_2 interface, the shallow defect could be in part associated to the amphoteric P_b center which can be found at the Si/SiO_2 transition.[59,60]

The analysis of the EIS measurements (see Section S1.5.2 of the ESI†) evidence a capacitive element characterized by a linear slope on the Mott–Schottky plot for reverse bias potential (Fig. 2c). The linear part indicates that the capacitive element originates from a potential distribution in the SCR for which the extracted donor concentration is in average $4.4 \pm 0.8 \times 10^{14}$ cm^{-3}. In Fig. 2d, it can be observed that the V_{bi} varies from 0 to 0.5 V while the V_{fb} spreads from −0.6 V to 0.5 V. Although negative V_{fb} have never been reported, such large V_{fb} variation have been observed in photo-electrochemical devices[20] but, to the best of the author knowledge, not in solid-state devices. A V_{fb} and V_{bi} correlation of ∼1 is obtained for $V_{fb} > 0$ V. In contrast for $V_{fb} < 0$ V, there is no correlation and the $V_{bi} \sim 0$ V for any V_{fb}. In the meantime, the *I*–*V* curves display a rectifying behavior (see Fig. S6†) with the derived V_{th} values being about 0.4 V for any V_{fb}. Although the V_{th} are considered less reliable due to possible leakage current (see the Section S1.5.3 of the ESI†), this value can correspond to the potential barrier generated by the interface states within the top 5–6 nm of the silicon, as interpreted from the PES measurements. The relatively constant V_{th} values might mean that the thermionic current is controlled by the potential barrier generated by the defects.

Fig. 3 displays the proposed potential distribution mechanism at the Si/SiO_2 interface unifying the PES with the electrical experiments providing information on the surface and the V_{bulk}, respectively. It is proposed that any increment in the external potential (Δ*V*), which can be realized in a change in the work-function of the contacted material ϕ_m or the bias potential V_g, is either distributed in the interface (Fig. 3a) under FLP or in the SCR once all the defects have been ionized (Fig. 3c). The last possibility is introduced as the Fermi Level Depinning (FLD). For instance, it can be realistic to assume that the FLP case described in Fig. 3a is encountered for $V_{bi} \sim 0$ V and $V_g > V_{fb}$ as evidenced by hatched part in Fig. 3g. In contrast, the FLD case described in Fig. 3c can be encountered for $V_g < V_{fb}$ and $V_{bi} \sim V_{fb}$ and corresponds to the linear part of the Mott–Schottky curve (Fig. 3i) as any potential increment fall in the SCR (Fig. 3f). Also, the measurements suggest that V_{fb} corresponds to the situation when the last interfacial defects is ionized[61] or to a shift in the potential distribution between the bulk, *i.e.* the space charge region (SCR), and the surface potential $V_{surf.}$ in the presence of interfacial defects (Fig. 3b). In other words, according to this study, the V_{fb} corresponds to the maximum $V_{surf.}$ for a flat V_{bulk} *i.e.* a flat SCR.

With regards to the results and their interpretation, the negative V_{fb} as observed in Fig. 2d are not erroneous. As represented in Fig. 3d, the negative V_{fb} should be considered as a proof that the interfaces are still subjected to the FLP for $V_g =$ 0 V with no potential distribution in the SCR (Fig. 3a). An additional bias potential must be applied to ionize all the interface states before any bias potential increment fall in the

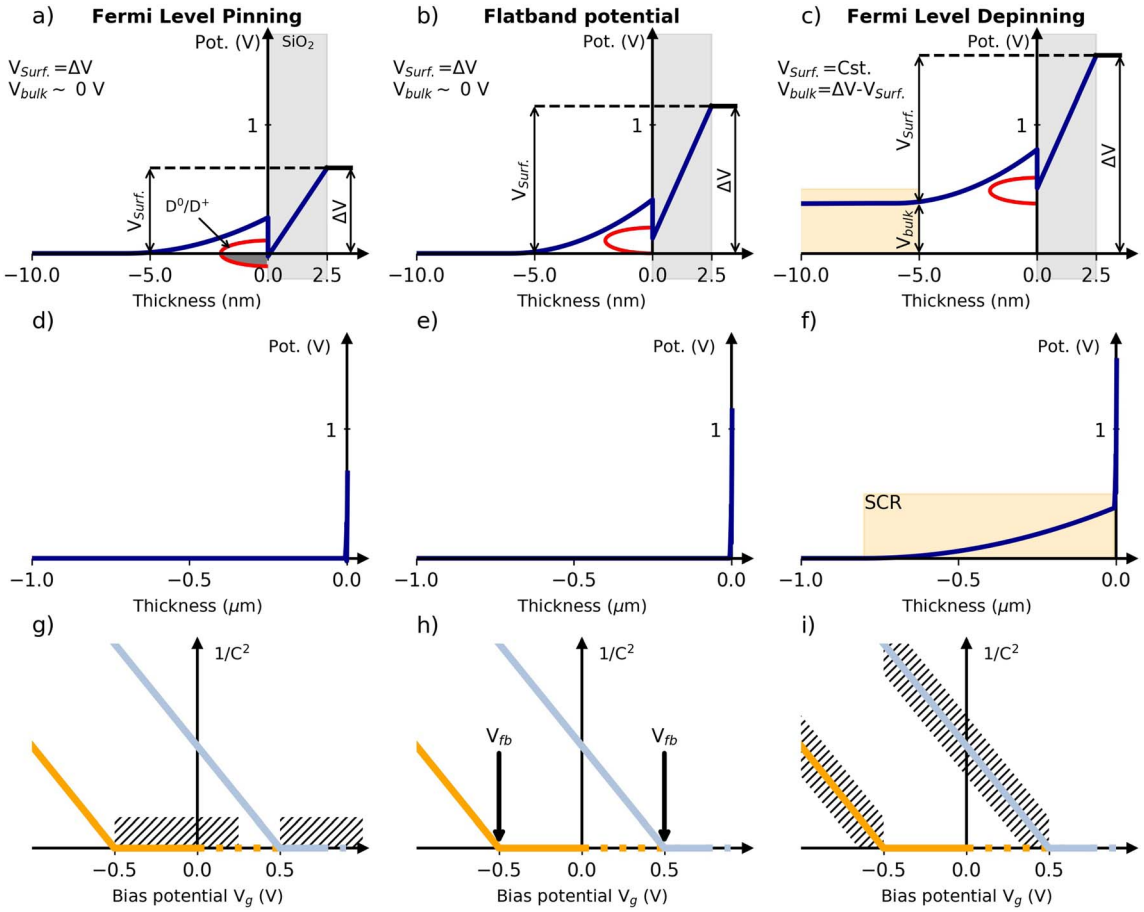

Fig. 3 Schematics of the proposed potential distribution between the $V_{surf.}$ and the V_{bulk} in the presence of a shallow interfacial defect (D^0/D^+) and a dipole at the Si/SiO_2 interface as resolved by the PES and the electrical measurements. $V_{surf.}$ during (a) Fermi Level Pinning (FLP), (b) the flatband potential (V_{fb}) and (c) Fermi Level Depinning (FLD). (d–f) are the V_{bulk} in the silicon under FLP, V_{fb} and FLD, respectively. The orange and blue Mott–Schottky curves are the same in (g–i) and are illustrative cases for a negative and positive V_{fb}, respectively. The hatched part of the Mott–Schottky curves in (g) and (i) corresponds to part subjected to the FLP and FLD, respectively. The annotation Cst. in (c) stands for constant. In the schematics, the dipole is constant for convenience but in reality it could vary in the course of the events.

SCR leading to the FLD case (Fig. 3c). The FLD can be also obtained when the difference $\phi_m - \phi_{sc}$ is large enough for ionizing all the interface states. Then, the measured V_{fb} is positive and is equal to V_{bi} measured for $V_g = 0$ V (see eqn (6)). It worths noting that the studied Si/SiO_2 interface provided a sharp transition between the FLP to the FLD case as $V_{surf.}$ is considered constant during the FLD (see Fig. 3c) because of the linear slopes in the Mott–Schottky plot (Fig. 2c) leading to the intrinsic donor concentration. However, it could be envisaged to find in other interfaces a shallow interfacial defect having a low state density and a large dispersion in the semiconductor bandgap, which could induce a competition between the V_{bulk} and $V_{surf.}$ even in large reverse bias. This case would result in a slope deviation from the ideal case in the Mott–Schottky plot.

From an electron affinity rule perspective, the workfunction of the n-Si(100) substrate can be estimated to be about 4.3 eV in taking $E_{CBM} - E_F = 0.3$ eV and an electron affinity of 4 eV (ref. 62) while the Pt and NiO workfunction are about 5.8–6 eV (ref. 63 and 64) and 5.2 eV if prepared under 200 °C,[65] respectively. The resulting workfunction difference $\phi_m - \phi_{sc}$ with the silicon can fall short to generate a built-in voltage *i.e.* a SCR, in the presence of a volt range $V_{surf.}$, as interpreted from the PES measurements. Therefore, the standard electron affinity rule described in eqn (1) can be refined in taking into account the quantity and the properties of interfacial defects in the generation of a surface potential ($V_{surf.}$):

$$qV_{bi}^{*} = \phi_m - \phi_{sc} - qV_{surf.} \quad (9)$$

In Fig. 2a, the FLP is observed by PES every time Pt is deposited on top of the Si/SiO_2, the $Si/SiO_2/Al_2O_3$ or the Si/SiO_2/NiO samples whereas the Si/SiO_2/NiO provides the largest Si^0 peak deviation. This can originate either from an induced photo-voltage during X-ray exposure[66] for the Schottky contacts providing $V_{bi} > 0$ V or because of the activation of additional defects interacting with the silicon bandgap[67,68] when $V_{bi} \sim 0$ V (see Fig. 2a and 3c). Also, the addition of an alumina layer on top of the Si/SiO_2 interface could generate a dipole[69–71] which compensates partially the surface potential drop induced by the defects at the Si/SiO_2 interface. Thus, the $Si/SiO_2/Al_2O_3$ structure

would be more favorable, under certain conditions of fabrication, to the build-up of a SCR in the silicon if Pt is deposited on top.

The large reported V_{fb} dispersion on the Si/SiO_2 interface in Fig. 2d can be explained by the numerous surface treatments and the degree of ionization of the detected shallow interfacial defects. Similarly, it can be expected that the potential profile induced at a photoelectrochemical system cannot only be influenced by the electrolyte composition such adjuvants and pH but also by the fabrication process, the surface termination and the interface engineering.[20,24,72–74] For this reason, a wide V_{fb} dispersion can be potentially reported for a single material in the presence of shallow interfacial defects. This explanation could hold for common metal-oxide semiconductor materials such as Fe_2O_3, TiO_2, SnO_2 and ZnO for which a volt-range V_{fb} dispersion is reported.[20,24]

Evidencing a defect induced volt range $V_{surf.}$ is not straightforward as the measurement techniques might be limited to the analysis of PES measurements in a contaminant free environment. Moreover, the obvious Si^0 and Si^{IV} PES peaks separation provided a prototypal interface to facilitate the analysis in term of potential distribution through the Si/SiO_2 interface which would not be the case for an homogeneous material. However, the literature indicates that the surface potential could be a key element for explaining some PES observations. For instance Lichterman *et al.* observed energetic surface effects with near ambient pressure PES measurements on TiO_2. Their presence were accompanied by a width increase of the PES peaks during the FLP and also in reverse bias potential during the Mott–Schottky measurements.[55] As for the Si/SiO_2 interface, it can be assumed that the FLP observed on the TiO_2 surfaces leads to the built-up of an important surface potential. Therefore, the presence of a $V_{surf.}$ driven by a shallow interfacial state and its implications on the V_{fb}, V_{bi} and V_{th} as well as the electron affinity rule could be valid for a wider class of semiconductor materials in both solid-state and photo-electrochemical devices.

Finally, standard quantities such as the V_{fb}, the V_{bi} and the V_{th} must be distinguished and manipulated with care considering that there are no straightforward correlations between these values (see Fig. 2d). It is shown in this study that the V_{bi} should be rather determined from the capacitive element associated to the SCR under zero current in the dark, as proposed in the eqn (6), and it is not necessarily correlated to the V_{fb}. Indeed, it is found that the V_{fb} is a quantity relating a shift from the FLP to the FLD case and is actually a potential for which the $V_{surf.}$ is maximal for a flat V_{bulk} in the presence of interfacial shallow defects subjected to an ionization reaction when the formation of an SCR in the semiconductor is attempted. This last definition does not contradict the current understanding of the flatband potential but adds a clarification in the case of a volt range defect-driven $V_{surf.}$ which is generally, if not always, ignored. This can explain the reported negative V_{fb} in this study and the large V_{fb} dispersion measured on different materials implemented in the photo-electrochemical devices. Also, the V_{th} can be substantially impacted by the barrier height at the very top nanometers in the semiconductor and does not display any correlation with the V_{fb} and the V_{bi}.

It is worth mentioning that V_{fb} reported in photo-electrochemical devices are not measured against a potential delivering a zero current condition but relatively to a reference electrode. This detail makes it difficult to evaluate the V_{fb} in term of potential distribution within the semiconductor materials. Therefore, it might be relevant to measure the V_{fb} in electrochemical systems against the open circuit voltage in absolute darkness which must be the potential delivering zero current.

4 Conclusions

This study combines PES and electrical measurements for probing the bulk (V_{bulk}) and the surface ($V_{surf.}$) potential at a tunneling Si/SiO_2 interface. The PES measurements highlights the presence of a substantial $V_{surf.}$ generated by shallow interfacial defects which can lead to a volt range potential drop within few nanometers. Standard quantities such as the V_{fb}, V_{bi} and V_{th} are extracted and compared between each other and also with the PES measurements. The analysis of the results evidence that correlation between the three mentioned quantities is not straightforward and therefore they must be manipulated with cares. The observed contradictions can be alleviated in considering the V_{bulk} relationship with the $V_{surf.}$ in the presence of shallow interfacial defects subjected to an ionization reaction when their energy level comes across the semiconductor Fermi level. Following this study, three recommendations can be provided for a better understanding of the semiconductor devices. First, the V_{bi} must be determined from the equivalent capacitive element related to the SCR under zero current conditions. Second, a defect-driven $V_{surf.}$ term must be included in the electron affinity rules which account for the experimental deviation from the theory. Third, the V_{fb} is actually a quantity expressing a flatness in the bulk of the material but not necessarily at the surface. With this clarification, a negative V_{fb} can be envisioned and it can explain the large V_{fb} dispersion reported in photo-electrochemical devices for a single semiconductor material. Also, the V_{fb} can be used for determining the potential regions under FLP to the regions under FLD but it should be defined relatively to the potential delivering a zero current condition for a better interpretation.

Author contributions

R. P. has designed and interpreted the experiments, and wrote the main manuscript as well as the ESI.†

Conflicts of interest

The author declares no conflicts of interest.

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